Design of Single Edge Triggered D Flip Flop Using GDI Technique

Hardeep Kaur[1], Sukhdeep Kaur [2], Er.Poonam Rani[3],
M.tech student,Dept,ECE, M.tech student,Dept.ECE, Assistant proff,Dept.ECE
Baba farid college of Engineering &Technology,Bathinda,Punjab,India

Abstract: *In cmos design goals ,cmos technology provides better results than TTL(Transistor Transistor Logic).but today due to increasing prominence of portable systems ,speed and low power designs are major issues in high performance digital systems .flip-flops are basic storage elements used in all kind of digital systems. Flip flops are widely used in memory elements, counters and registers also. And these circuits are used to implementation of vlsi chips. So power consumption is the major concern in this which should be improved. This paper proposes a a Design of single edge triggered low power d Flip Flop using GDI(Gate Diffusion Input Technique).As a result using GDI power consumption is Reduced and features the best power delay product. The operation of the D flip flop is analyzed and simulated using Tanner EDA .*
Keywords- *GDI Technique, negative edge triggered D flip flop, power, High speed.*

I. Introduction

Now a day, with the increasing use of Mobile devices, laptops, consumer electronics demand a stringent constraint on reducing power dissipation. Flip flops are the key elements used in sequential digital systems. Flip flops and latches are the basic elements for storing information. Flip flop is one of the most power consumption component. Flip flop is the most important state holding elements. Several flip flops was researched and presented. In this paper an efficient technique is presented. .D flip flop is implemented using GDI (Gate diffusion input)is introduced. Using GDI the main attention has been in improving the performance of the circuit and reduced power delay product. There are two types of d flip flops are found in literature that are single edge triggered and double edge triggered .but the double edge triggered flip flops suffers from performance degradation, because it samples data on both clock edges. The single edge triggered flip-flops are simple in design and sample data only one clock edge(either positive or Negative).These are mostly designed by using master slave configuration.

II. GDI Function

Gate diffusion technique is defined as a new technique of low power digital combination of circuit design. This allows reduced power consumption and delayed propogation.The GDI technique is more important because it involves only two transistors. GDI technique can be used to design fast , low power circuits using only few transistors and reduced power consumption ,delay and area of the digital circuit. It maintains low complexity of logic design.GDI Technique is very flexible for digital circuits and power efficient using less transistor count.GDI method is based on the simple cell. That is shown in figure .1. It contains four terminals, G node, P node and N node are inputs and D node is output. G node is the common gate input of PMOS and NMOS. P node is the outer diffusion node of PMOS.N node is the outer diffusion node of NMOS. D node is the common diffusion of both transistors P, N,D may be used as input or output depends upon the structure requirement.
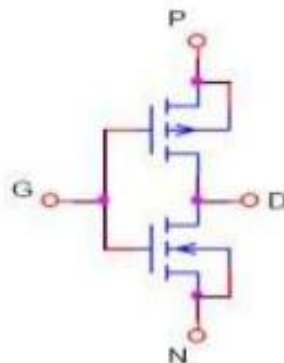

Fig.1 GDI Cell

It should be noted that the source of PMOS in GDI cell is not connected to VDD or source of NMOS is not connected to GND. This feature gives the GDI cell two extra input pins to use to makes the GDI design more flexible than conventional methods.

There are some functions that can be implemented by GDI Technique.

N	P	G	D	FUNCTION
'0'	B	A	A*B	F1
B	1	A	A+B	F2
'1'	B	A	A+B	OR
B	O	A	AB	AND
C	B	A	AB+AC	MUX
'0'	1	A	A	NOT

The advantage of GDI cell is the any logical functions can be implemented easily than other conventional methods.

III.   GDI Flip Flop Implementation

An implementation of low power negative edge triggered D flip flop using GDI (Gate Diffusion Input) technique. The main aim of this work to minimize the power dissipation using GDI Technique. It is called Gate Diffusion Input Technique because the inputs are directly diffused into the gates of the transistors of N type and P type devices. This Negative edge triggered D flip flop is designed using Master slave configuration and both contains four GDI cells, and the sampling is done on the falling edge of the clock signal. In this the input at the falling edge is transferred to output port. Body gates and inverters are used in this circuit. Body gates used for creating two alternative paths as for holding state or transparent state and inverters are used for buffering of the internal signals for swing restoration .This circuit contains 18 transistors including inverters .so it is an efficient alternative for low power consumption and better performance than conventional methods. Figure. 2 shows the GDI D flip flop implementation circuit .
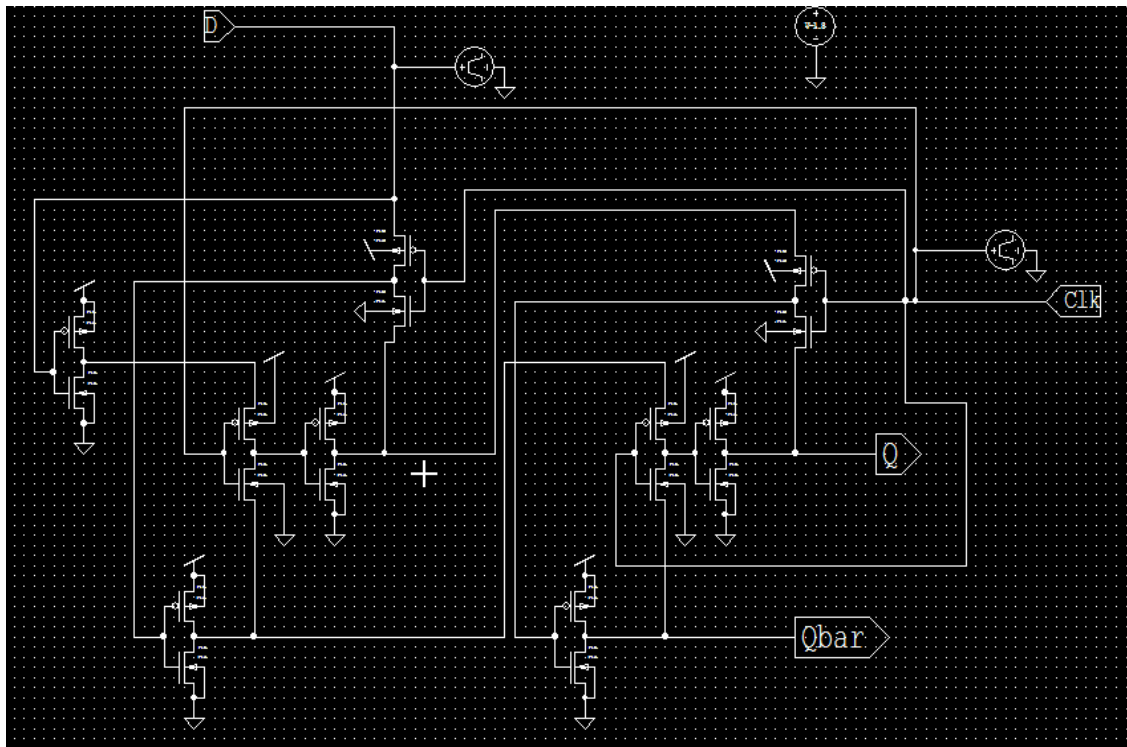

Fig.2 GDI based D flip flop implementation

IV.   Simulation Results

In this circuit implementation is done using L= 0.18u,w= 0.36u for NMOS and L= 0.18u, W= 0.72u for PMOS .The circuit was simulated using 1.8 v for 180 nm technology. According to these values the simulation output waveform for negative edge triggered D flip flop as shown below in figure.3.
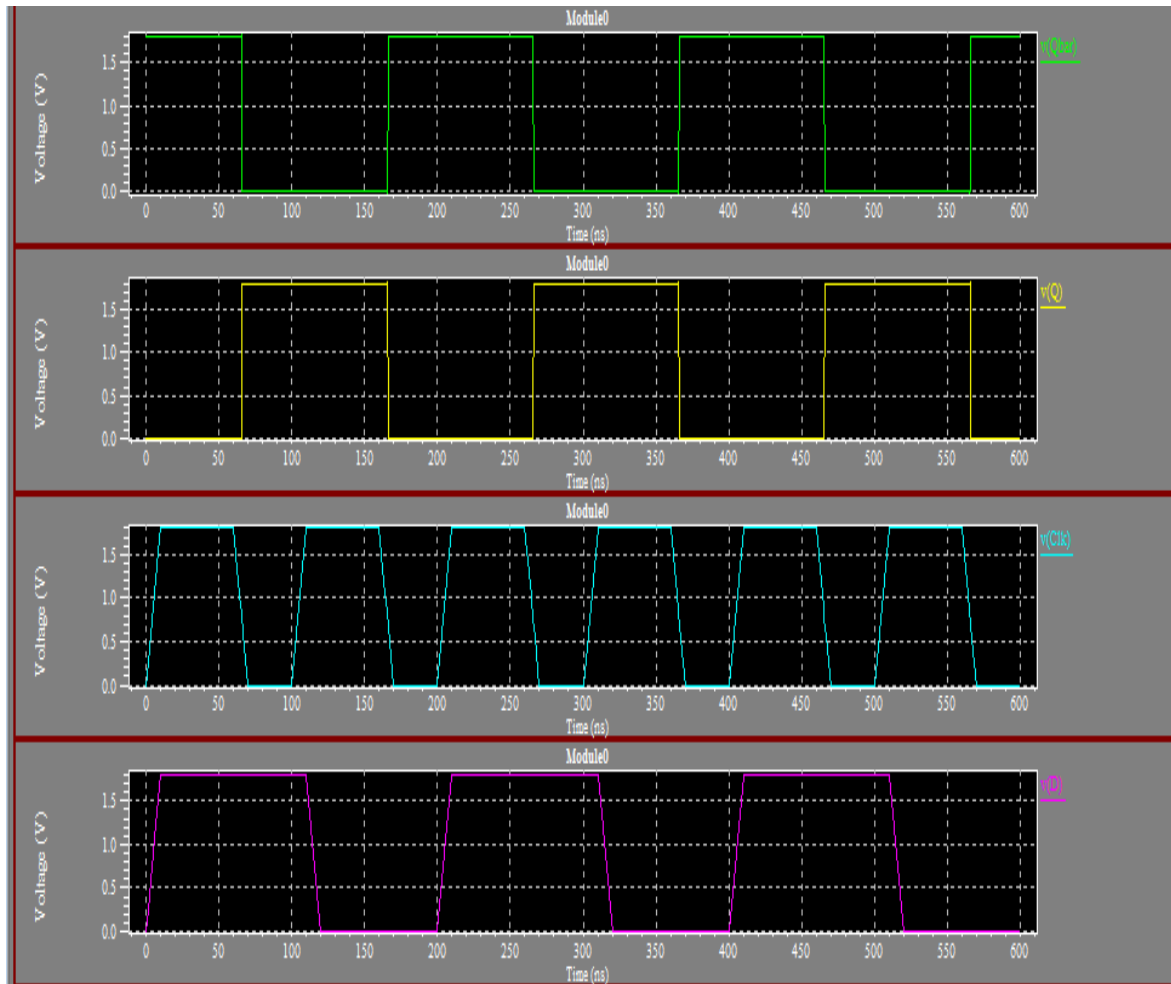
Fig .3. GDI based D flip flop Output waveform

V.   Final Results Using Gdi Technique

Circuit	#no of transistors	Length Of PMOS	Width of PMOS	Length of NMOS	Width of NMOS	Avg. Power	Max. Delay
GDI	18	0.18u	0.72u	0.18u	0.36u	1.77 uw	5.48ps

Table.1- Simulation results for o.18um technology

The simulation results shows in Table .1. The power disipation reduced 40% then conventional methods and it includes 18 transistors. Minimum power and delay produced by sizing, if transistor count less than size is also small and power will be less consumed.

VI.   Conclusion

In low power applications, power consumption and area are the main aspects to design over other methods. So using GDI Technique power consumption is less than other methods and transistor count is also less. This negative edge triggered D flip flop shows better performance and design is simulated using 180 nm technology. It is suited for low power applications and used for high performance design.

References

[1].   Vladimir Stojanovic and vojin G.oklobdizia,Fellow IEEE, Comparative Analysis of Master Slave latches and flip flops for high performance and low system ,IEEE journal of solid state circuits ,vol.34,No.4 April 1999
[2].   Arkadiy Morgenshtein, Alexander Fish and Israel A,Wagner, Gate Diffusion Input- A power efficient method for digital combinational circuits, IEEE Transactions very large scale integration(VLSI) systems,vol.10,No. 5 October 2002
[3].   Kuo-Hsing Cheng and Yung- Hsinang Lin, A dual pulse clock double edge triggered flip flop for low voltage and high speed applications,IEEE,2003
[4].   Arkadiy Morgenshtein, Alexander Fish and Israel A,Wagner, An efficient implementation of D flip flop using GDI Technique, IEEE 2004

[5]. M.W.phyu,W. L Goh and K.S Yeo, A low power Static dual Edge triggered Flip flop using an output controlled Discharge configuration, IEEE 2005

[6]. Yu Chien- Cheng, Design low poer double edge triggered flip flop circuit, IEEE 2007

[7]. Manoj Sharama, Dr. Aarti noor, shatish Chandara Tiwari, Kunwar singh, International conference on Advances in recent Technologies in computation and computing ,IEEE 2009

[8]. Jin-fa Lin, Ming-Hwa Sheu and Peng-siang Wang, A low power dual mode pulse Triggered flip flop using Pass transistor logic, IEEE 2010

[9]. Wing –shan Tam, Sik-Lam siu,Chi wah kok and Hei wong, International conference of Electron Devices and solid state circuits, IEEE 2010

[10]. K.G Sharama ,Tripti Sharama , B.P singh and Manisha sharama, Modified Set D flip flop Design for Low power Vlsi applications.IEEE 2011

[11]. Panshul Dobriyal, Karna sharama,Manan Sethi ,Geetanjli Sharma, A high performance D flip flop Design with low power clocking system using MTCMOS Technique, IEEE 2012

[12]. Y.syamala, K.Srilakshmi and someshkar varma, Design of Low power CMOS logic circuits using Gate Diffusion Technique,international Jouranal of VLSI design & communication systems (VLSICS) ,vol. 4,No. 5,October 2013,

[13]. N.Vishnu Vardhan Reddy, C.Leela mohan & M.srilakshami, GDI based subthreshold low power D flip flop,International jouranal of VLSI and Embedded system,2013

[14]. Amit Grover , Sumer singh, D flip flop with different Technologies, Advanced engineering technology and application,2014

[15]. Jin –Fa Lin, Low power pulse triggered Flip flop design based on a signal feed Through Scheme, IEEE Transactions on very Large scale integration (VLSI) systems ,Vol.22,No.1.Januarary 2014.